Using Chaos to Broaden the Capture Range of a Phase-Locked Loop: Experimental Verification

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Abstract — In this paper, we present and discuss some circuit experiments that verify our previous claims, which were based on numerical simulations of mathematical models, that chaos can be used to broaden the capture range of the common phase-locked loop circuit.

1 Introduction

Chaos can be used to broaden the capture range of a phase-locked loop. This nonlinear dynamics-based aided-acquisition technique uses an external modulating input to throw the unlocked loop onto a dense chaotic attractor that overlaps the original capture range. When the state of the circuit nears the capture point — the point where the circuit would reach equilibrium if it were locked to that input — the chaos-inducing modulation is turned off and the loop's original dynamics capture the signal.

The roots of this approach lie in work by Chua *et al.*[7, 8] and D'Humieres *et al.*[5] on chaos in the phase-locked loop, as well as in more-recent research in the nonlinear dynamics community on controlling chaos, ably summarized in [14]. An early instance of innovative and intentional use of chaos in electronic systems was Pecora and Carroll's work on synchronized chaos and its use as a communications technique[4, 12]. Several schemes that exploit chaos to effect design improvements in circuits — the phase-locked loop[2], associative and random-access memory[1], and the delta-sigma modulator[13], among others — have been proposed in the last few years. This paper presents some experimental results that verify the theoretical analysis and numerical experiments in the first of those four applications.

The phase-locked loop circuit used in the experiments reported here can be easily constructed with standard ICs. The topology is similar to that of the basic phase-locked loop found in any textbook, but includes an extra modulating input that can be used to force the circuit into chaotic behavior. For each circuit, we measured the capture and lock ranges $\Delta\omega_C$ and $\Delta\omega_L$, then randomly chose a frequency ω_{test} outside the former and inside the latter — a frequency that an unaided, unlocked loop could not otherwise acquire. We determined a set of modulation parameters $\{A_d,\ \omega_d\}$[1] that, in conjunction with ω_{test}, induce a chaotic attractor that covers the phase-space point where the circuit would equilibrate if it were locked to ω_{test} (i.e., if the reference frequency started out *inside* $\Delta\omega_C$ and then moved smoothly and slowly up to ω_{test}). Since a chaotic attractor is covered densely by any trajectory in its basin of attraction, all points upon it — most importantly, the *capture point* defined in the previous sentence — are *reachable* from all points in that basin. The time required to reach a point on a chaotic attractor is by definition nondeterministic, as it is sensitively dependent upon the exact initial conditions; the implications of this are discussed later in this paper. When the trajectory nears the capture point, a comparator circuit clears a flipflop, removing the external modulation and allowing the circuit's original dynamics to lock on to the signal. The enforced tolerance of the match — the size of the *target box* around the capture point within which the comparators fire — has several obvious implications and a few less obvious ones, which are summarized in the next paragraph and discussed in more detail in section 3.

Overall, the results were consistent with our previous predictions[2] — this technique can indeed effectively broaden the capture range of the circuit. We verified the effects over several hundred trials under a variety of conditions. In each, we set the reference input to ω_{test}, applied a sinusoidal signal $A_d \sin \omega_d t$ to the modulation input, waited until the target flipflop cleared, and determined whether or not the loop had indeed locked. When the target was small, enforcing a close approach along the chaotic attractor to the capture point, lock was reasonably reliable (86-94% success rate, depending on the relative position of the test frequency inside the capture range) and fast (within a few cycles of the reference input). The 6-14% failures were caused by mismatches in phase and frequency. The latter, a result of nonzero target size and approach tolerance, caused the success rate to degrade in the predictable way with increasing target size. Phase mismatches were corrected with an added phase-monitoring device, bringing the lock success rate to 96-100%. Both effects are discussed in detail in section 3.

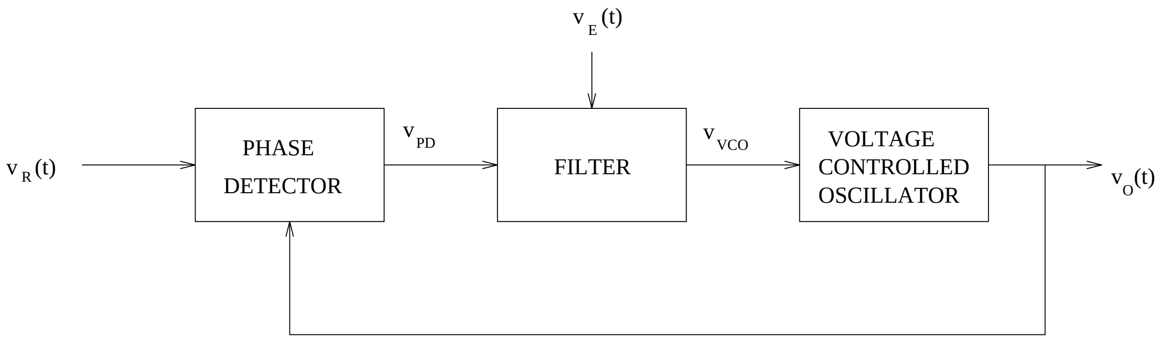

Figure 1: Phase-locked loop block diagram

The next section briefly outlines the theory of the phase-locked loop and presents some corroborating results on chaos and modulation in the circuit. The theoretical and numerical analysis of this system appears in a previous paper[2] and is not duplicated here. The following section explores chaotic lock and capture in more detail.

2 Chaotic Behavior of the Phase-Locked Loop

The block diagram of the phase-locked loop (PLL) used here is shown in figure 1. The mathematics of this system and of its chaotic behavior, summarized in this section, are covered in more detail in [2]. The phase difference $\Delta\phi$ between the reference input $v_R(t)$ and the output $v_O(t)$ of the circuit's internal voltage-controlled oscillator (VCO) is measured, filtered, and used to drive the output frequency of the VCO in the direction that minimizes $\Delta\phi$ and synchronizes the output and input frequencies. The phase detector (PD), which measures $\Delta\phi$, is the source of the nonlinearity that causes the system's chaotic behavior. The VCO input voltage and the PD output voltage are the state variables of the system. Phase detectors can take on a variety of forms. We chose the sample-and-hold (S&H), described in detail in [2] and in [5]. This circuit has significant advantages and drawbacks: it is common in the literature and yields clear oscilloscope photos, but is difficult to analyze. The simple mixer is common in textbooks, much easier to analyze, and difficult to observe in the phase space. The loop filter, normally used to remove harmonics from the signal, has a second input in this circuit, labeled $v_E(t)$ in the figure. This topology is often used to modulate a second signal onto a carrier wave. Here, v_E is used to selectively drive the loop into a chaotic regime.

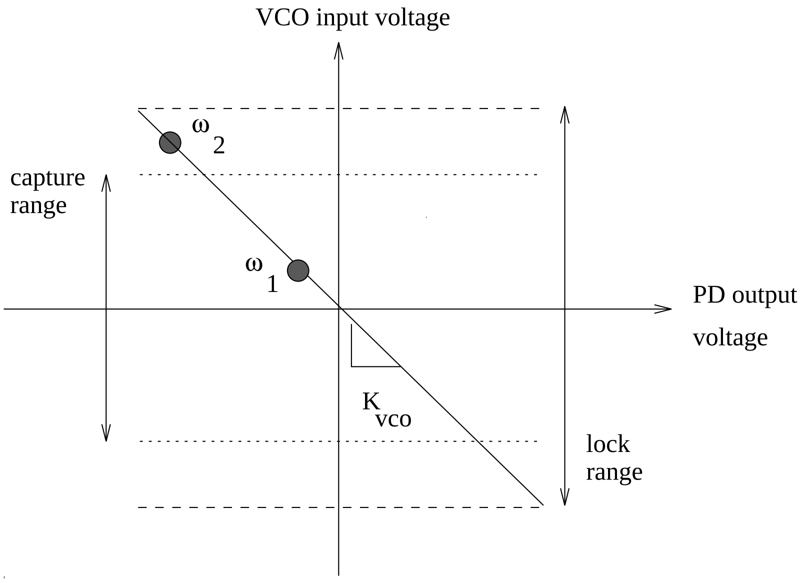

Figure 2: Phase-space diagram of lock range, capture range, and circuit state. State variables are the voltages labeled V_{PD} and V_{VCO} in the previous figure.

Presented with an input whose frequency ω_1 is near the *center* or *free-running* frequency $\omega_\odot$ of the VCO, the PLL synchronizes its output accordingly:

$$v_O(t) = A \sin(\omega_1 t + \phi_{\Delta 1})$$

where A is the (fixed) amplitude of the VCO. A DC voltage at v_{VCO} is required to offset the VCO from $\omega_\odot$ to ω_1. The feedback loop settles to the constant phase difference $\phi_{\Delta 1}$ that provides this offset:

$$v_{VCO} \cdot K_{VCO} = \omega_\odot - \omega_1$$

where K_{VCO} is the VCO gain factor in radians per second per volt. If the PD is a simple mixer, its output is proportional to the sine of the phase difference:

$$v_{PD} = K_{PD} \sin \phi_{\Delta 1}$$

where K_{PD} is the PD gain factor in volts per radian. The nonlinear transfer function of the S&H PD is significantly more complicated; see [2] for more details. If the input frequency to a locked loop is changed smoothly and slowly, lock can be maintained out to the edges of the *lock* or *tracking* range, $\Delta\omega_L$, which is generally determined by the hard limits of the VCO. Figure 2 shows these relationships schematically. Note that the diagonal line on this figure would be inverted if the polarity of the VCO were reversed.

If, on the other hand, the frequency of the input to an unlocked loop is *not* close to $\omega_{\odot}$, the frequency of the PD output can exceed the cutoff frequency of the filter, effectively breaking the feedback path. This, together with other effects, both linear and nonlinear, limits the *capture* or *pull-in* range $\Delta\omega_C$ to a narrower frequency band than $\Delta\omega_L$. It also means that the circuit can only reach the point labeled ω_2 in figure 2 via the diagonal line *starting from a locked state inside the capture range*. The nonlinearity of the PD vastly complicates the calculation of $\Delta\omega_C$; until recently, few general results were available and textbooks contained disclaimers like "a general expression for loop capture range is not available as the system is highly nonlinear[16]." Chapter 5 of Gardner's classic work on the PLL[9] gives a good summary and history of this type of analysis. Tanaka *et al.*[17] have very recently begun to apply techniques from nonlinear dynamics to this problem, yielding some interesting and useful results.

Figure 2 and the previous discussion cover the theoretical relationships between lock range, capture range, circuit state, and VCO and PD gain factors. The rest of this section reports on the actual behavior of the circuit. When the loop is locked to some input reference frequency ω_i, the state of the circuit is quiescent somewhere inside the dashed lock range limits on the diagonal line of figure 2, verified experimentally in the circuit via the voltage measurements graphed in figure 3. Part (a) of figure 4 shows an oscilloscope photo of one point on this line. The edges of the capture range of this circuit — the dotted lines in figure 2 — were measured at 100.8kHz and 102.3kHz. Outside this range the circuit cannot completely track the phase difference. The shortfall, a highly nonlinear function of the waveforms involved, propagates around the loop, yielding the deformed ellipse shown in part (b) of figure 4. A similar picture results, but for different reasons, if a *locked* loop is modulated with a small, low-frequency voltage, as shown in figure 5(a). This ellipse is more regular than the curve in part (b) of figure 4 because the circuit is cleanly tracking the small sinusoidal phase difference introduced on the v_E input, rather than oscillating in a nonlinear fashion. As either the modulation frequency or amplitude is raised, analysis and simulations[2] predict bifurcations to higher-order limit cycles, followed by chaotic behavior. Part (b) of figure 5 shows a photograph of the circuit after such a bifurcation has occurred, causing the period-one limit cycle of part (a) to become a period-two limit cycle[2]. Figure 6 shows two views of a chaotic attractor at a yet-higher modulation frequency. Part (a) is a real-time image of the trajectory as it

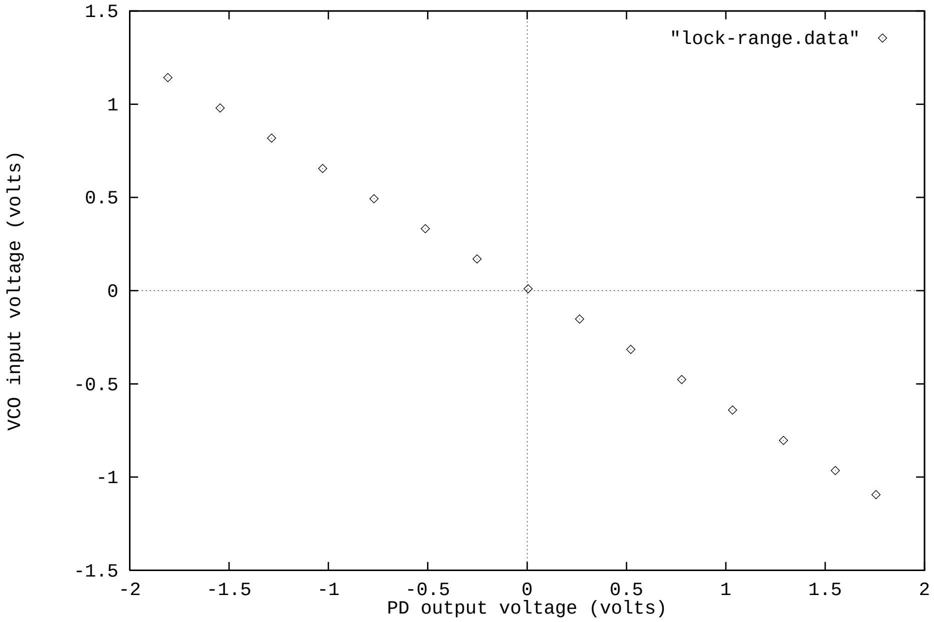

Figure 3: Locus of measured equilibrium states in locked loop: VCO input voltage versus PD output voltage

Figure 4: Phase-locked loop (a) locked to a 102kHz reference input and (b) unsuccessfully attempting to lock to a 104kHz reference input. (Axes: VCO input voltage versus PD output voltage.)

Figure 5: Phase-locked loop locked to a 101kHz reference input and modulated with (a) 350Hz, 0.2V signal (b) 408Hz, 0.2V signal. (Axes: VCO input voltage versus PD output voltage.)

covers the attractor; in part (b), a Poincaré section, v_E is connected to the oscilloscope's trigger input, strobing the trajectory once per drive period and revealing the fractal structure of the chaotic attractor. This is precisely the type of attractor that is used in the capture range-enhancing experiments reported in the next section.

3 Forcing Capture with Chaos

To use a chaotic attractor to make a phase-space point reachable, one must not only find a range of parameter values that create such an attractor; one must find the precise values, such as $\{A_d = 0.2,\ \omega_d = 2\pi(386.7)\}$ in figure 6, that force it to cover that particular point. Because chaotic attractors occupy nonzero phase-space volumes, and because they respond in at least partially predictable ways to changes in parameters, this task is not difficult; in fact, it has been automated in a computer program that uses computer vision, geometric phase-portrait analysis, and other artificial intelligence-based techniques[3].

To apply chaos-induced reachability to the PLL, we find chaotic attractors that touch the capture point — the point on the diagonal line of figures 2 and 3 — for every

Figure 6: Phase-locked loop locked to a 101kHz reference input and modulated with 386.7Hz, 0.2V signal: (a) trajectory (b) Poincaré section. (Axes: VCO input voltage versus PD output voltage.)

anticipated input frequency. When an out-of-range input is detected, the appropriate drive is applied to the modulating input and the resulting chaotic trajectory is monitored until it approaches the corresponding capture point. The modulation is then removed, allowing the circuit's original dynamics to lock on to the input. Because of its reliance on the lock-in dynamics, this technique cannot broaden the capture range beyond the original lock range limits. This approach is similar in spirit to some existing aided acquisition techniques, such as Gilchriest's use of random noise to cause the state of an unlocked circuit to "hunt" around for an otherwise-unaccessible target point[10]. Our approach is different in that it uses *deterministic* dynamics, wherein the introduced signal and its effects on the phase-space structure can be predicted and analyzed.

One of the apparent weaknesses of chaos-induced reachability is that, in contrast to Gilchriest's added-random-noise approach, it requires input frequencies to be known in advance, planned for, and recognized in real time. Upon first examination, it appears that this scheme would require one to find and store an infinite number of $\{A_d,\ \omega_d\}$ pairs, one for each point in the range between $\Delta\omega_C$ and $\Delta\omega_L$. This is not the case. Because of attractor volume and deformation properties, a single set of modulation parameters create an attractor that is suitable for chaotic capture over a *range* of input frequencies — usually a wide range and often even the *entire* range between $\Delta\omega_C$ and $\Delta\omega_L$, making this drawback moot.

Chaos's special properties have both good and bad implications here. Since trajectories densely *and nondeterministically* cover chaotic attractors, reachability is provable, but the delay may be long — or even infinite. Because of the hallmark *sensitive dependence on initial conditions*, one can only make stochastic statements, based on ratios of target areas to the area of the entire attractor, about the time to acquire lock. This extreme sensitivity, however, is not uniformly disadvantageous. It does not threaten the existence or structure of the attractor because of the stability implied by the shadowing lemma[11, page 251], informally stated thus: "with high probability, the sample paths of the problem with external noise follow *some* orbit of the deterministic system closely[6]." In fact, sensitive dependence can even be exploited as leverage by suitably intelligent control schemes[3, 15].

The general form of the PLL to which we applied these techniques is shown in the block diagram in figure 1. The PD was based on a 398H sample-and-hold and a 4098 one-shot[3]. The center frequency $\omega_\odot$ of the VCO, an Exar XR2206, was set to approximately 101.5kHz with a 1000pF capacitor and the lock range was measured as [98.1 - 105.2kHz]. The RC-lowpass filter cutoff frequency was approximately 1kHz and the capture range was measured at [100.8 - 102.3kHz], as mentioned previously. See the appendix for a detailed block diagram and schematic of the circuit.

To verify that chaos can be used to force capture of an input that would otherwise be out of range, we used three different input test frequencies ω_{test} between $\Delta\omega_C$ and $\Delta\omega_L$ — one at each end of the frequency gap and one in midrange, so chosen in order to explore whether the capture/lock dynamics varied across that range. For each ω_{test}, we determined the capture point: the equilibrium locked-state values of the PD output and VCO input voltages, the variables that define the state of the circuit and the axes of the phase-space plots in the figures and photographs in this section. The three test frequencies and the corresponding capture points are shown in the first three columns of table 1. We then searched for a set of drive parameters — amplitudes and frequencies for v_E — that combined with the loop's inherent dynamics at each ω_{test} to create a chaotic attractor that overlapped the corresponding capture point. These values are shown in the two right-hand columns of table 1. Attractor classification and parameter-

ω_{test} (Hz)	Capture Point		Drive Parameters	
	v_{PD} (volts)	v_{VCO} (volts)	A_d (volts RMS)	ω_d (Hz)
98.5	1.551	-0.965	0.4	431
99.3	1.230	-0.770	0.67	209
100.5	0.522	-0.315	0.71	99

Table 1: Test frequencies, the capture points for those frequencies, and the drive parameters that create chaotic attractors covering those capture points

ω_{test} (Hz)	Target Size	Low Corner (v_{PD}, v_{VCO}) (volts)	High Corner (v_{PD}, v_{VCO}) (volts)
98.5	small	(1.609, -1.02)	(1.617, -1.005)
98.5	medium	(1.600, -1.036)	(1.63, -0.992)
98.5	large	(1.577, -1.063)	(1.652, -0.969)
99.3	small	(1.226, -0.774)	(1.24, -0.764)
99.3	medium	(1.197, -0.792)	(1.261, -0.743)
99.3	large	(1.168, -0.811)	(1.286, -0.726)
100.5	small	(0.600, -0.39)	(0.608, -0.39)
100.5	medium	(0.583, -0.394)	(0.62, -0.37)
100.5	large	(0.567, -0.416)	(0.642, -0.35)

Table 2: Target box sizes

space exploration were done by eye and by hand, respectively; again, this process can be automated using phase-portrait analysis techniques[3]. The criterion used to classify chaos was the presence of apparent fractal phase-space structure[4]. A bank of comparators was programmed to detect when the state of the circuit neared each capture point, to within the three tolerances listed in table 2. The comparators' output cleared a flipflop, removing the external modulation and causing the system to revert to its original dynamics.

Figure 7 shows a digitizing oscilloscope trace of the entire process described in the previous paragraph. The top trace is a gating signal whose low-to-high transition initiates the acquisition scheme and the bottom trace is the phase-detector output. After traveling on the attractor for roughly half a cycle, the trajectory enters the target box, causing the comparator circuit that detects the chaotic trajectory's proximity to the acquisition point to fire, thereby removing the chaos-inducing modulation. The circuit then locks on to the previously out-of-range input.

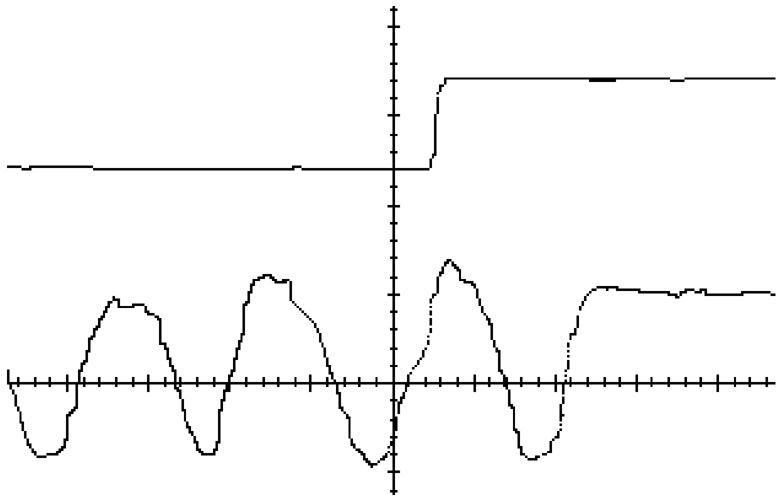

Figure 7: Oscillograph of chaos-aided acquisition: the top trace is a gating signal whose low-to-high transition initiates the acquisition scheme and the bottom trace is the phase-detector output. After traveling on the attractor for roughly half a cycle, the trajectory enters the target box, causing the comparator circuit that detects the chaotic trajectory's proximity to the acquisition point to fire, thereby removing the chaos-inducing modulation. The circuit then locks on to the previously out-of-range input. Scale: vertical 5V/div, horizontal, 5ms/div

When the comparators fire, the state is not precisely at the capture point — unless the target size is zero, which would require an infinite acquisition time. A larger target thus hastens acquisition, but introduces mismatches, from which the circuit cannot always recover. In this particular set of several hundred experiments, delay was not a problem; the trajectory always reached the target within a few cycles of ω_{test}. Since mismatches cause problems and acquisition was so rapid, small targets would seem most appropriate for practical application of this technique. However, the small but finite probability of a long acquisition time should be factored into the design decision. One would not wish to use chaos-aided acquisition in a time-critical part of an avionics system, for instance.

The effects of frequency mismatches are apparent in the third column of table 3, which gives lock success rate as a function of target size, both with and without phase mismatch compensation, which is described later in this section. As expected, the success rate degrades as the target grows, since the frequencies can differ by as much as the target width multiplied by K_{VCO}. It does not, as one might expect, degrade smoothly as the test frequency moves away from the capture range boundary; rather, the success rate is highest in the *middle* of the band between $\Delta\omega_C$ and $\Delta\omega_L$. One possible explanation

ω_{test} (Hz)	Target Size	Lock Success Rate Without Phase Compensation	With Phase Compensation
98.5	small	91%	97%
98.5	medium	86%	
98.5	large	77%	
99.3	small	94%	100%
99.3	medium	90%	
99.3	large	89%	
100.5	small	86%	96%
100.5	medium	77%	
100.5	large	74%	

Table 3: Lock success rates over 100 trials, for different target sizes, both with and without phase mismatch compensation (capture range: [100.8 - 102.3 kHz])

for this is some sluggishness or memory in the circuit's response. Unless the response is instant, the direction of approach into the target box will affect the success rate: if the trajectory approaches from the capture range side, the circuit may retain some vestiges of its capture-range dynamics, aiding the capture process. Testing this would require systematic construction of several overlapping chaotic attractors for each ω_{test} and observation of various secondary patterns in the flow of trajectories across the target box and in the success rate results. We are currently investigating this.

Frequency mismatch is not the only cause of failure. The *phases* can also differ — by as much as $\pm\pi$, depending on the relative timing of the comparator transition and the input zero crossing. To assess the effects of this, we performed a series of experiments to determine how much phase step a locked loop could withstand. The results are shown in figure 8. All of the frequencies in the figure lie between the capture and lock range limits — the band between the dashed and dotted lines of figure 2. Across the entire range, the circuit tolerates more negative than positive phase step, an effect corroborated in [5]. Predictably, the phase-step tolerance is lowest near the lock range end of the band and highest near the capture range, approaching $\pm\pi$ at the edge of $\Delta\omega_C$.

Extending the results in figure 8 to explain the effects of phase mismatch in a chaotically hunting loop requires a few stochastic approximations. Near the capture range, the chaotic loop can tolerate more phase step — both in locking and in staying locked. Since this mismatch depends on the acquisition time along the chaotic attractor, it too

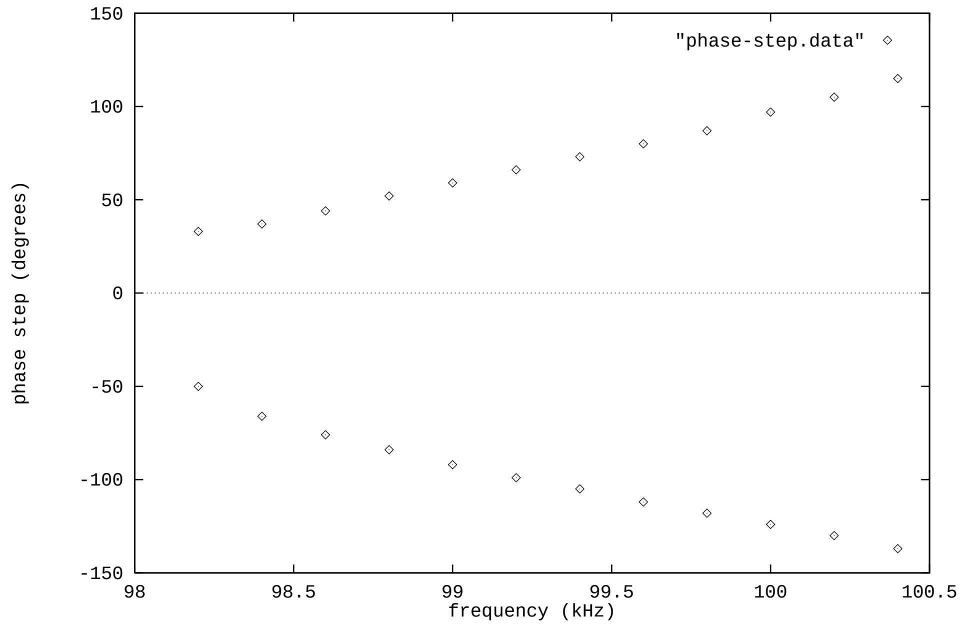

Figure 8: The maximum phase step that a locked loop can withstand, as a function of frequency. The edge of the lock range is 98.1kHz and the edge of the capture range is 100.8kHz

is sensitively dependent on initial conditions; one can only make stochastic statements about its distribution, and then only if *frequency* mismatch effects can be neglected, which is not the case here. The obvious solution to the phase mismatch problem is to measure phases as well as frequencies. We did so by narrowing the pulse in the PD that samples the input phase, gating it with the comparator output, and using this signal, instead of the raw comparator output, to clear the target flipflop. Since the gated signal only allows the target flipflop to clear near the zero crossing of the input waveform, the phases are roughly equal. This improves the success rate dramatically, as can be seen in the last column of table 3, and was not accompanied by any significant increase in the acquisition time. Further improvements could be effected with some sort of anticipatory control, based on the derivatives and perhaps integrals of the trajectory. Another way to improve the scheme would be to analyze the patterns in the attractor threads more carefully and adjust the modulation parameters so as to situate dense attractor regions near the capture point. Ideally, of course, one could create a small chaotic attractor that is completely contained in the target box, in which case acquisition would be fast and 100% successful.

Incidentally, if the target size is infinite — that is, if the chaos-inducing drive is removed at an arbitrary time in the cycle — the lock success rates over 100 trials are 6, 13, and 54% for ω_{test} = 98.5, 99.3, and 100.5Hz, respectively. Even without a defined and detected target, the chaotic drive aids acquisition by nudging the trajectory, on the average, towards the capture point. However, the target comparators are necessary to make this approach truly useful.

4 Conclusions

Chaos can be used to selectively make phase-space points *reachable*. One interesting and potentially useful application of this is to broaden the capture range of the phase-locked loop out to the original lock range limits. This paper presents physical experiments that verify some previous theoretical and numerical studies of this idea.

For the entire range in question — where the loop would otherwise be unable to lock — we were able to construct chaotic attractors that overlapped the capture points. The comparator circuit reliably detected the system trajectory's proximity to those points and removed the chaos-inducing modulation, causing the loop to lock on to the newly in-reach inputs. As expected, the success rate degraded with the size of the target within which the comparators fired, since larger targets leave larger frequency mismatches for the loop to overcome when the drive is turned off and the original dynamics take over. Some counterintuitive patterns also emerged in these frequency mismatch effects. One would expect the loop to be able to tolerate more mismatch near the capture range than near the lock range, but the performance was best in the middle of the frequency band between the two. This probably stems from memory effects in the circuit and the direction of approach along the chaotic attractor into the target box (i.e., from the lock range side or the capture range side), and thus is a function of the global structure of the chaotic attractor. Phase mismatches also caused lock failure, but in a more-predictable pattern, and so were easily overcome with an additional phase-monitoring device, raising the lock success rate significantly.

This technique is robust. The percentages in the data tables reflect the results of hundreds of trials in several versions of the circuit, all built with ordinary, imprecise electronic components. This stands in direct conflict with the common conception of chaos as a sensitive and unpredictable phenomenon. The resolution to this apparent paradox lies in the way that it is used here: we exploit its characteristic structure (e.g., denseness of chaotic attractors; the stability implied by the shadowing lemma; see section 2) and work around its disadvantages (e.g., nondeterministic acquisition time), insofar as possible. The close corroboration of numerical and analytical predictions and experimental results verifies our previous statements about the robustness of the approach, which also extends to the equations: the circuit model used to derive the equations in [2] subsumed a variety of assumptions: for example, that the reference input, modulating input, and VCO output are pure tones at fixed amplitudes, that the PD is effectively linear in the VCO's range, etc. None of these assumptions appear to have affected the success of the predicted outcome.

The goal of this paper was to experimentally validate the notion that chaos can be used to improve a circuit's design. This particular circuit could have been improved in other ways, particularly since we require the input frequencies to be known in advance. For instance, one could use a switched-capacitor filter or a voltage-controlled resistor to adapt the bandwidth of the loop filter to the sensed input frequency. One could also adjust the center frequency of the VCO — and thus the capture range — by adding a DC or random offset to the VCO[5]. Using chaos to broaden this range is simply a new and different slant; it provides a possible solution when, for example, a set of design criteria are for the most part easy to meet, but are vastly complicated by one outlying requirement. Consider a loop that must acquire lock very quickly, with no overshoot, in a small range of medium frequencies, and that must *also* lock to some other, much smaller, frequency, *with acquisition time being of little consequence.* In this case, one might design the loop around the first cluster of requirements using standard techniques, then use the methods described in this paper to bring in the outlying point.

Chaos-induced reachability is powerful and useful. It has a wealth of potential applications in all branches of engineering, especially because chaos is so common, in both natural and man-made systems. However, because of its drawbacks — nondeterministic acquisition time, for instance — the solution proposed here is by no means universal.

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A Block Diagrams and Schematics

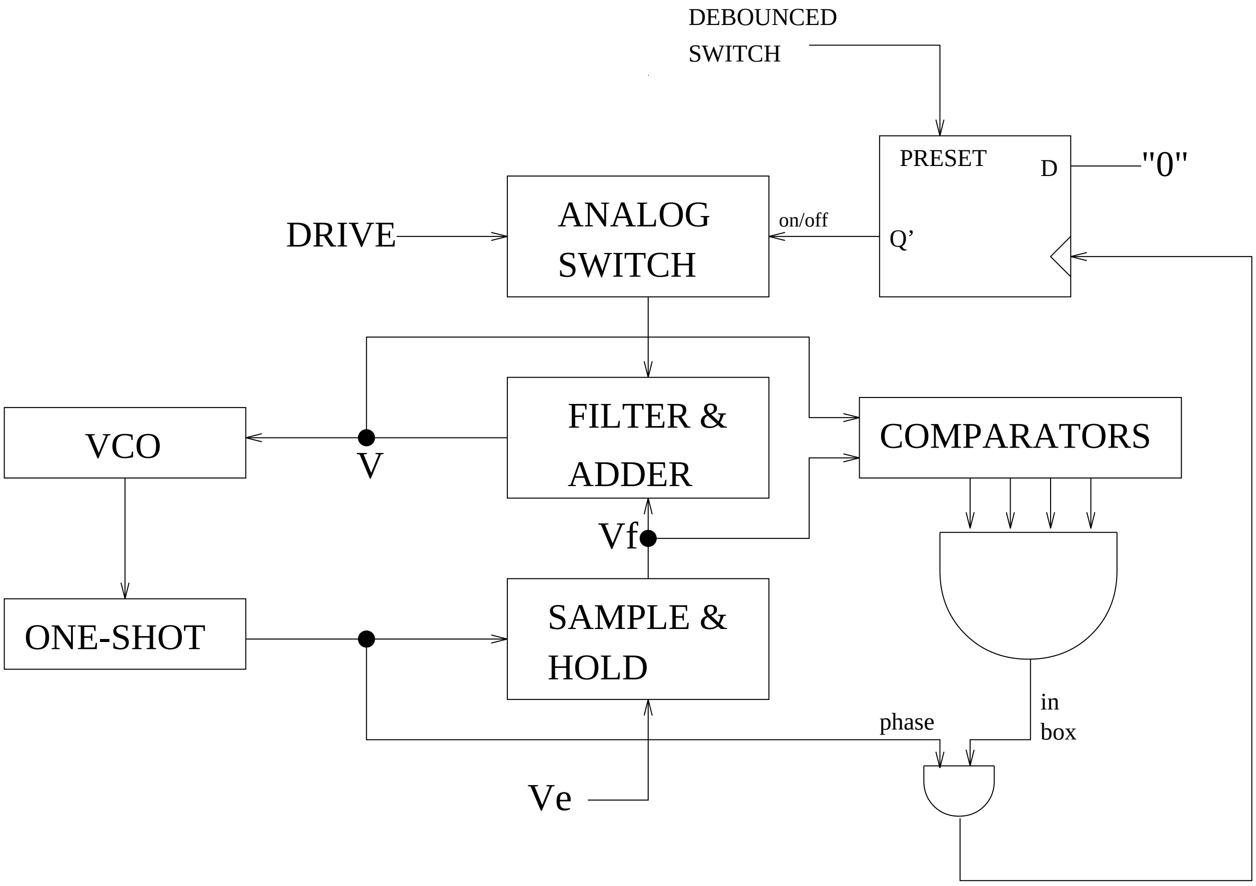

Figure 9: Block diagram of the phase-locked loop

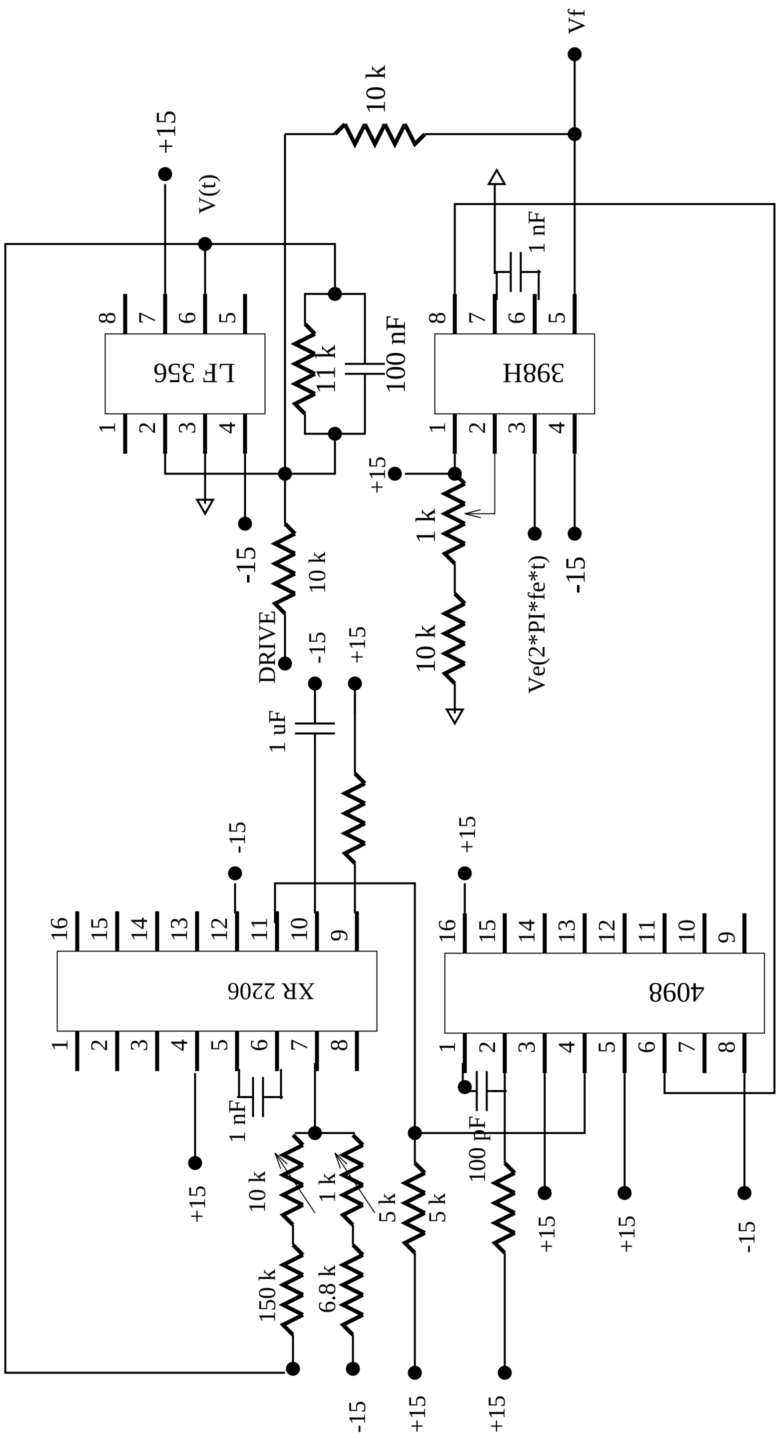

Figure 10: Schematic of the phase-locked loop

Footnotes

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[1]the amplitude and frequency of the modulating input

[2]The trace makes one circuit of this attractor in every two drive periods.

[3]The latter fires at the zero crossings of the VCO output voltage, causing the former to sample the input and effecting a direct measurement of the phase difference.

[4]The rigor of this often-used heuristic is a topic of some debate in the dynamics community.

[5]The latter is essentially the approach taken by Gilchriest, as discussed in section 2.

Figure and Table Captions

Fig. 1. Phase-locked loop block diagram

Fig. 2. Phase-space diagram of lock range, capture range, and circuit state. State variables are the voltages labeled V_{PD} and V_{VCO} in the previous figure.

Fig. 3. Locus of measured equilibrium states in locked loop: VCO input voltage versus PD output voltage

Fig. 4. Phase-locked loop (a) locked to a 102kHz reference input and (b) unsuccessfully attempting to lock to a 104kHz reference input. (Axes: VCO input voltage versus PD output voltage.)

Fig. 5. Phase-locked loop locked to a 101kHz reference input and modulated with (a) 350Hz, 0.2V signal (b) 408Hz, 0.2V signal. (Axes: VCO input voltage versus PD output voltage.)

Fig. 6. Phase-locked loop locked to a 101kHz reference input and modulated with 386.7Hz, 0.2V signal: (a) trajectory (b) Poincaré section. (Axes: VCO input voltage versus PD output voltage.)

Fig. 7. Oscillograph of chaos-aided acquisition: the top trace is a gating signal whose low-to-high transition initiates the acquisition scheme and the bottom trace is the phase-detector output. After traveling on the attractor for roughly half a cycle, the trajectory enters the target box, causing the comparator circuit that detects the chaotic trajectory's proximity to the acquisition point to fire, thereby removing the chaos-inducing modulation. The circuit then locks on to the previously out-of-range input. Scale: vertical 5V/div, horizontal, 5ms/div

Fig. 8. The maximum phase step that a locked loop can withstand, as a function of frequency. The edge of the lock range is 98.1kHz and the edge of the capture range is 100.8kHz

Fig. 9. Block diagram of the phase-locked loop

Fig. 10. Schematic of the phase-locked loop

Table 1. Test frequencies, the capture points for those frequencies, and the drive parameters that create chaotic attractors covering those capture points

Table 2. Target box sizes

Table 3. Lock success rates over 100 trials, for different target sizes, both with and without phase mismatch compensation (capture range: [100.8 - 102.3 kHz])

Biographies

Elizabeth Bradley received the S.B., S.M., and Ph.D. degrees from the Massachusetts Institute of Technology in 1983, 1986, and 1992, respectively, including a one-year leave of absence to compete in the 1988 Olympic Games. She joined the Department of Computer Science at the University of Colorado at Boulder in January of 1993 as an Assistant Professor, with a joint appointment in Electrical and Computer Engineering, and is also affiliated with the Program in Applied Mathematics and the Department of Mechanical Engineering's Combustion Center. Her research interests are nonlinear dynamics and chaos, scientific computation and AI, network theory and circuit design, and classical mechanics. She is a member of Eta Kappa Nu, Tau Beta Pi, and Sigma Xi, and the recipient of a National Young Investigator award and a Packard Fellowship.

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Douglas E. Straub received his B.S. degree in electrical engineering from Rice University in 1992. He is currently pursuing his Ph. D in electrical engineering at the University of Colorado.

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Photos attached.